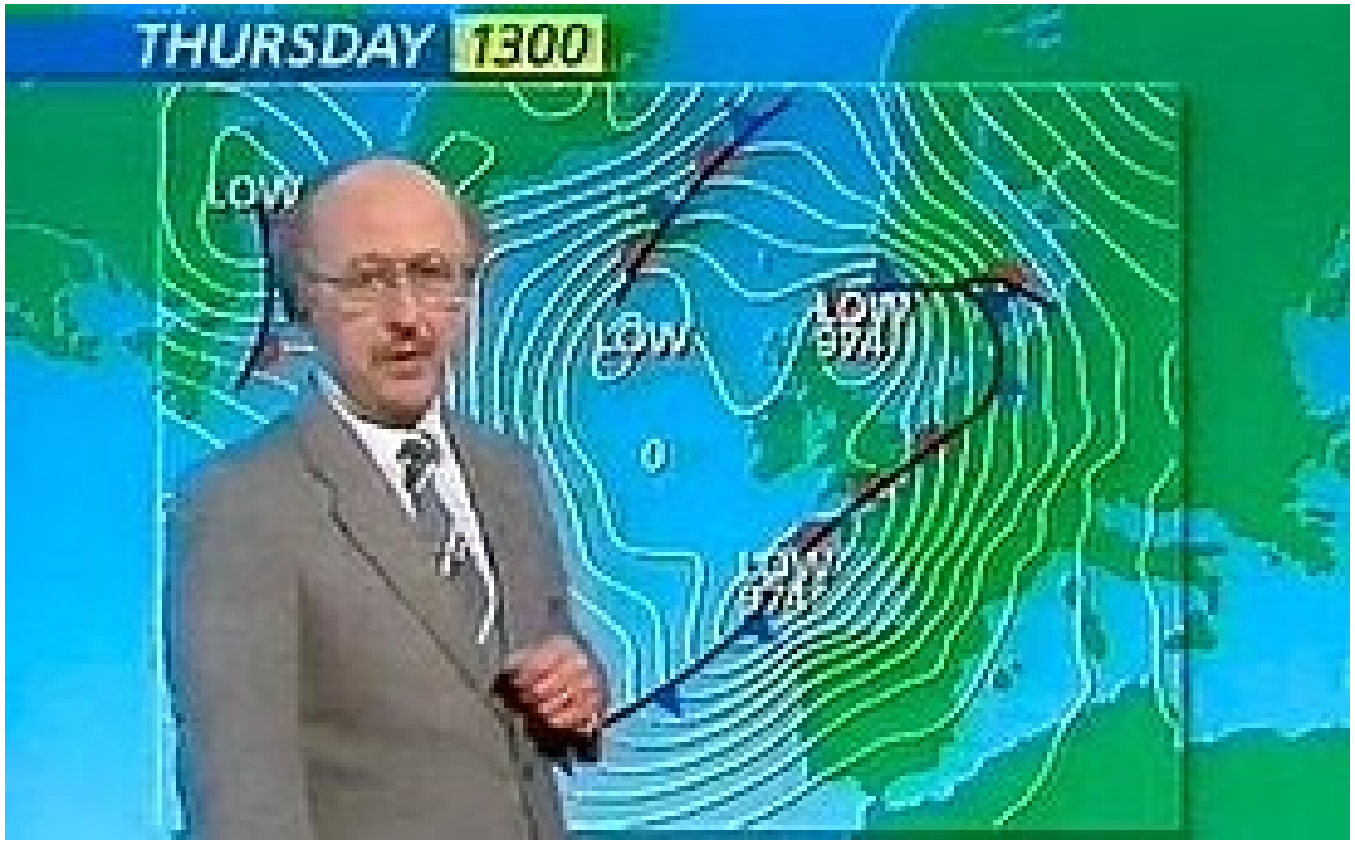
Inventing Actionable Intelligence

Embedded Tech Trends 2020

Nigel Forrester

October 1987 – BBC Weather Report

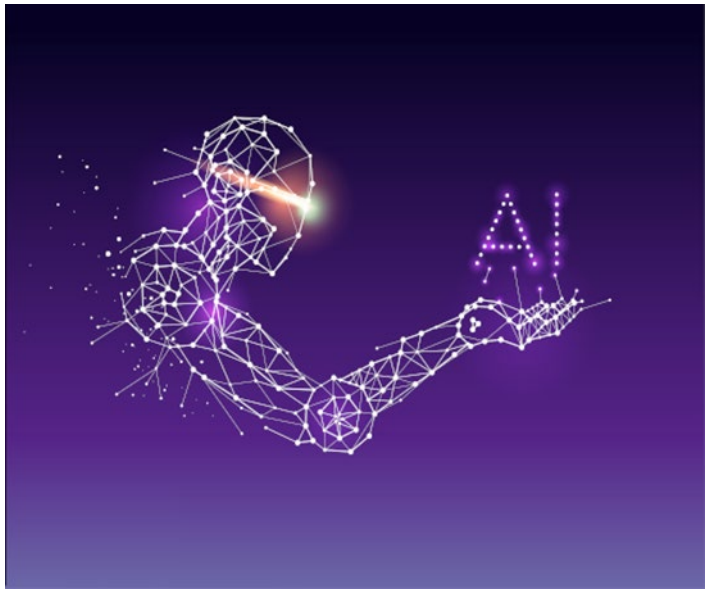


Courtesy: BBC

- Was the intelligence correct?
- Was it interpreted correctly?
- Could the intelligence have been useful?

Data Analysis Techniques

- The amount of data is growing exponentially
- We have some very comprehensive traditional methods to interpret it
- Artificial Intelligence (AI) provides a different insight
- Inference at the Edge is the application of AI at the point of interest



RF SigInt Applications

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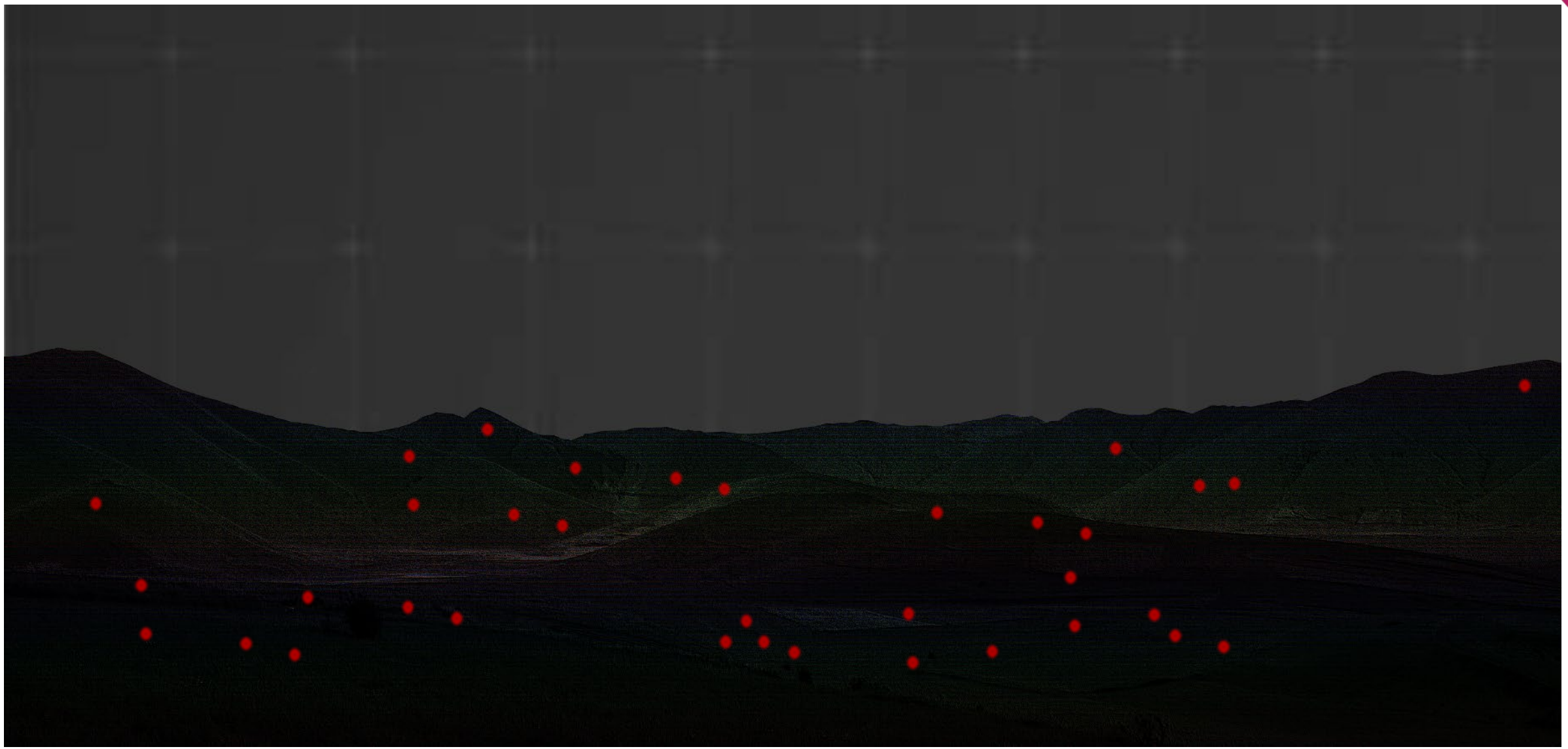
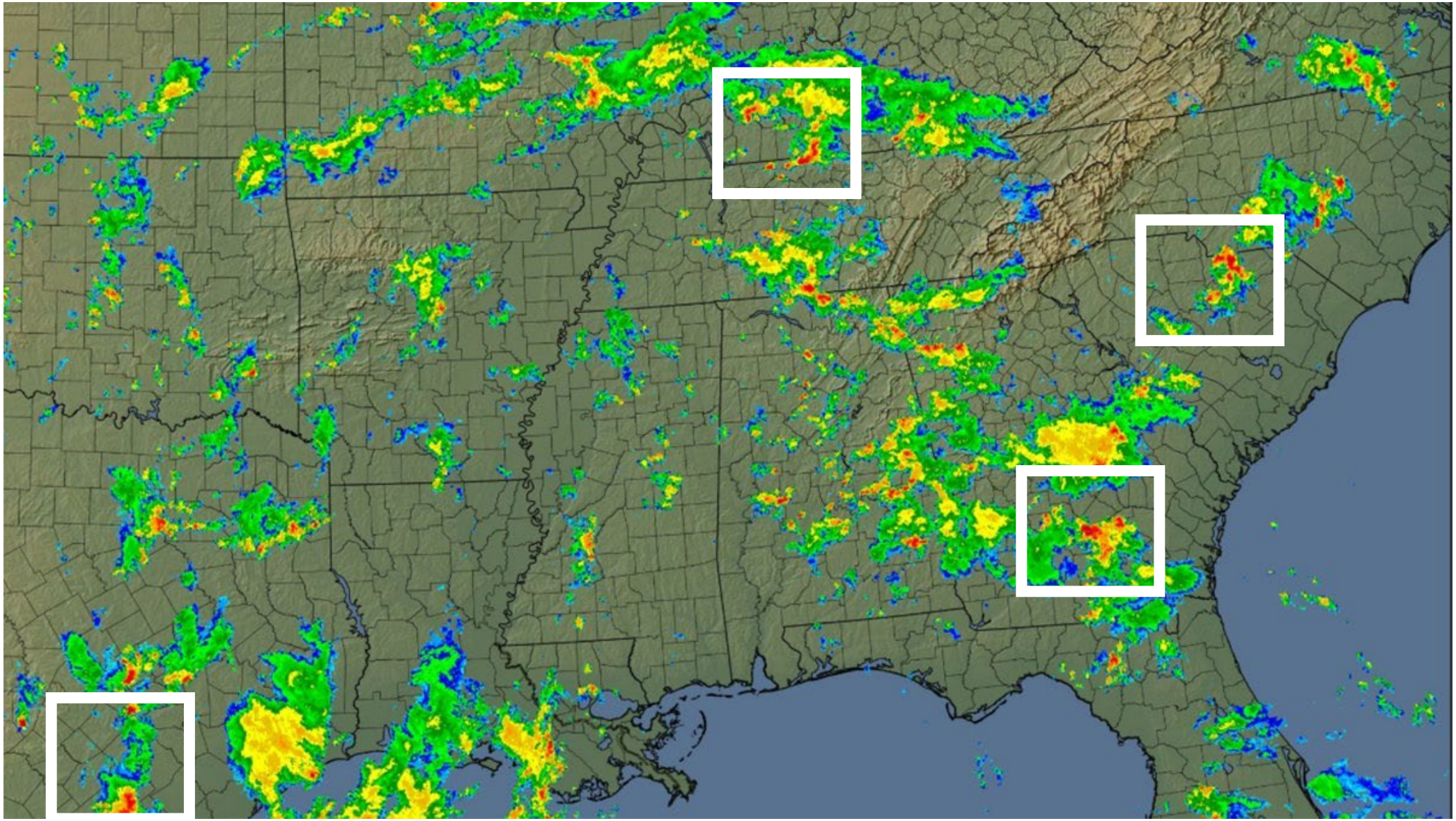


CPU Board for Inference at the Edge Applications

- Key requirements include:
  - Maximize the number of cores and memory
  - Make suitable for deployment in extreme environments
  - High bandwidth interfaces
- TR J4x/6sd-RCx is our latest processor offering with:
  - 12-cores, 64GB DRAM, 2TB storage
  - Rugged conduction-cooled only
  - Supports latest OpenVPX™ profiles
  - 40G optical interface used to input high bandwidth IQ data from RF front end in VITA 49 format

VITA 66.5 Style B or C compatible in position P2A with MM12 MT location A

RADAR Applications



RADAR Applications (cont)

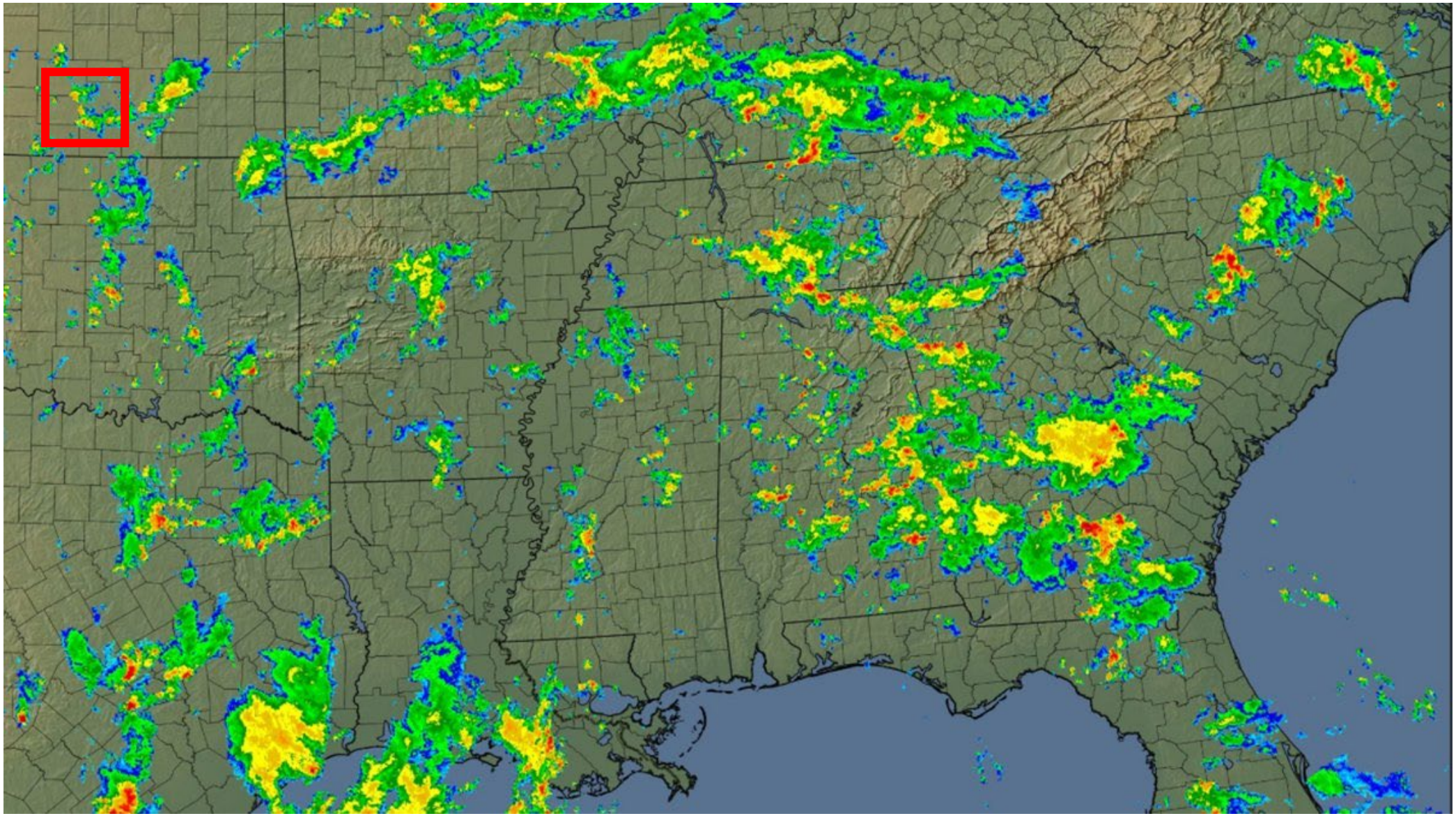
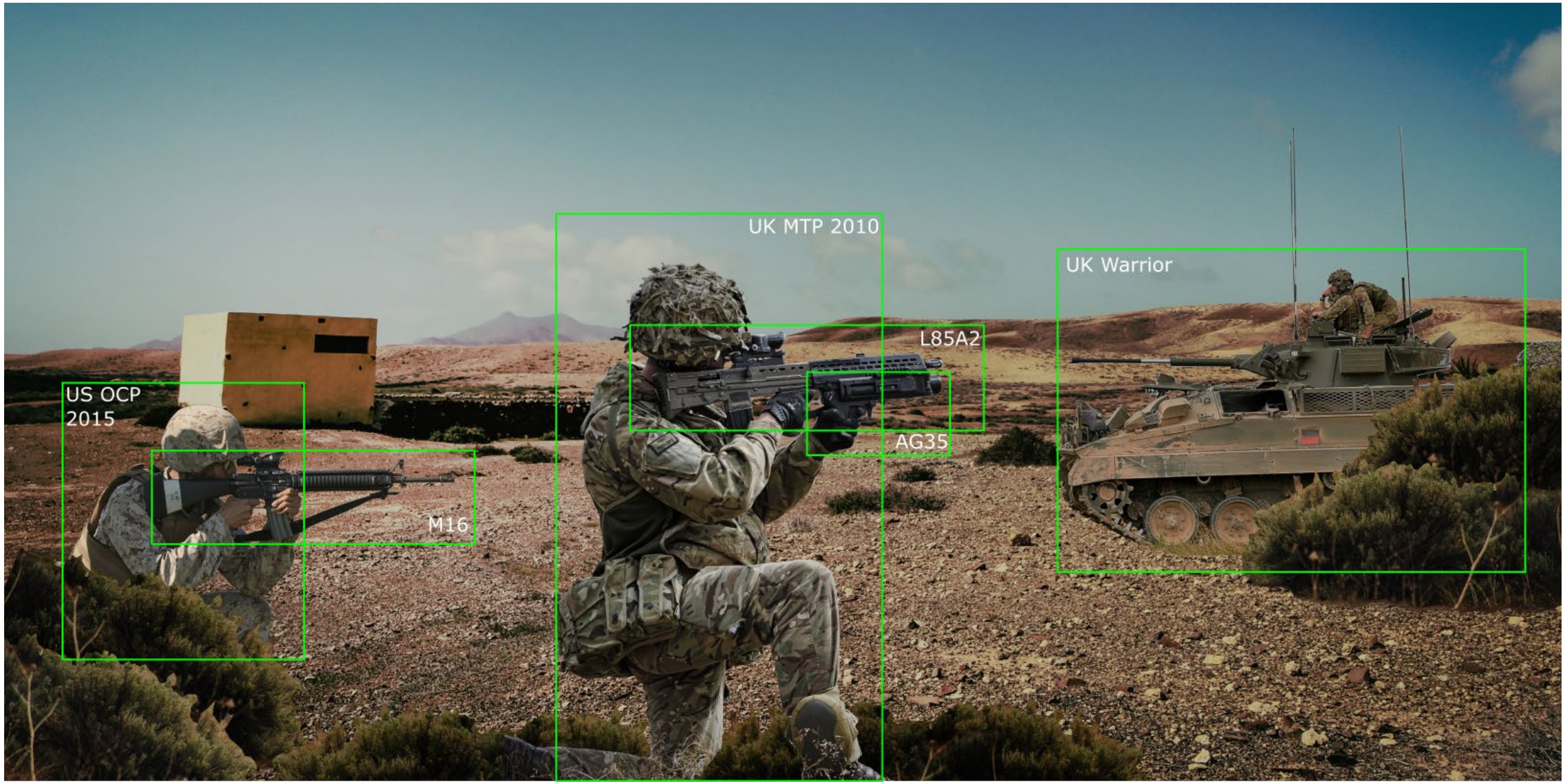
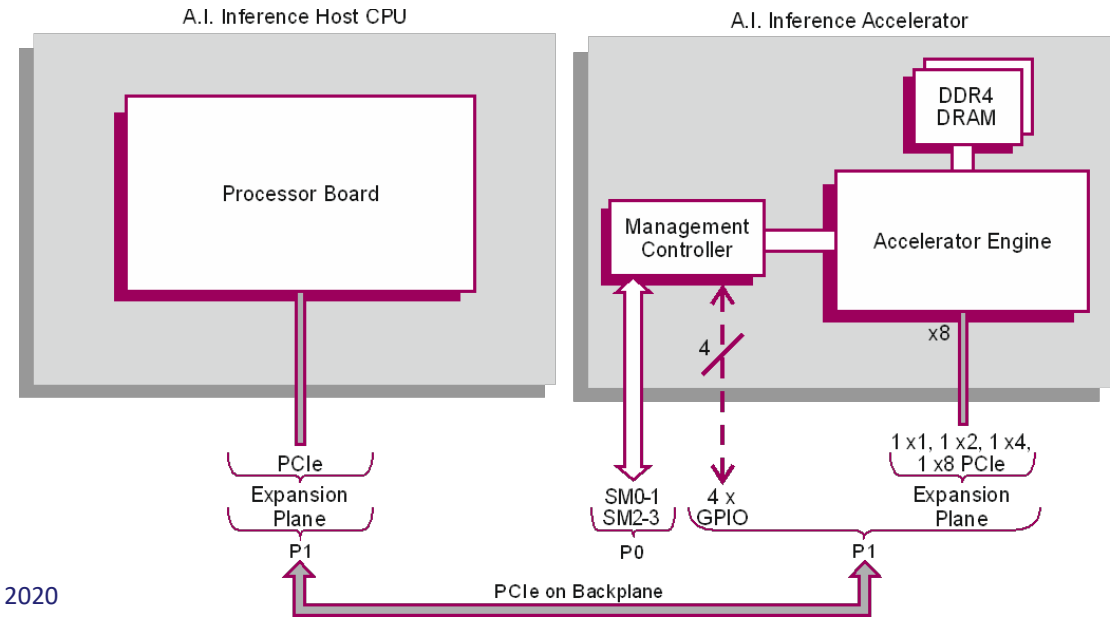


Image and Video Applications



AI Accelerator Engine

- PCIe Gen 3 connection to host
- Neural network models supported including AlexNet, ResNet, SqueezeNet, GoogleNet, MobileNet
- Deep learning primitives supported including Convolution, Fully Connected Layer, Rectified Linear Layer, Local Response Normalization, Max and Average Pooling, Concatenation and more
- Using frameworks including TensorFlow, Caffe, MXNet



Higher Performance Processing with Heterogeneous Resource Pool

CPU Only

CPU + FPGA

CPU + 2 FPGA

Benefits

- Relatively easy to try an existing network model and framework in a deployable environment
- Overall performance can be decent but power consumption can be challenging
- Some performance optimizations possible including:
  - Development of custom primitives
  - Tweaking layer flow between CPU and FPGA
  - Minimize model size

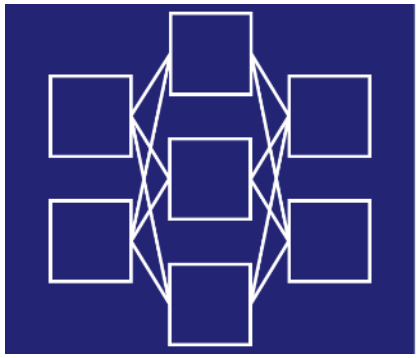
Fully Optimized Solution

- Requires time to optimize the model
- We will be providing an OpenCL BSP and the necessary tools to do this

FPGA only

An example to end

Wolf



Dog

Dog

Wolf

Thanks